REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Upon entry of this amendment, claims 1 ,3, 5-9, 11-16, 18-21, and 23-31 will remain in the application.

Claim Rejections - 35 USC § 103

Claims 1 ,3, 5-7, 9, 11-14, 16, 18-20, and 23-31 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Shang et al. (U.S. Patent No. 5,941,980, hereinafter "Shang") in view of Iizuka (U.S. Patent No. 5,299,321) and in further view of Scantlin (U.S. Patent No. 5,574,927).

Claims 8, 15, and 20 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Shang in view of Iizuka and in further view of Scantlin, and further in view of art described in the Specification at page 1, line 19 to page 2, line 2.

Neither Shang nor Iizuka disclose or teach emulation. The Action relies on Scantlin for a teaching of emulation. However, the emulation taught by Scantlin is not for testing, but rather to emulate an instruction set for a target computer to execute software written for the target computer (e.g., a legacy system) on a computer with a different instruction set. Thus, "emulation", as used by Scantlin, is directed to operational compatibility between different computer architectures.

Applicants teach emulation for testing and debugging one computer architecture rather than compatibility between differing architectures. The system taught by Applicants utilizes a testing interface to provide instructions from an in-circuit-emulator (ICE) to an emulation instruction register capable of holding multiple instructions to be issued to the

processor pipeline during an emulation operation (Specification at page 8, line 12 to page 9, line 3 and page 10, line 20 to page 11, line 2).

The testing interface described in the application, the JTAG interface, is defined by the IEEE 1149.1 standard and has a specific protocol. In typical systems, only one instruction is issued through the test interface at a time, and no new instructions are issued until a run-test-idle (RTI) state signal is received (page 11, lines 14-19). However, Applicants teach loading multiple instructions through the test interface into the emulation instruction register at a time to avoid the need to enter the RTI state, which requires a clock cycle, and thus, slows down the emulation operation (page 10, line 20 to page 11, line 2).

The Action states that Scantlin describes the JTAG testing interface, citing col. 4, line 34 to col. 5, line 27 and Figure 2. However, the term "JTAG" does not occur in the cited section, Figure, or anywhere else in the patent according to a word search of the document. Scantlin does not teach issuing instructions through a test interface during an emulation, let alone issuing multiple instructions through a test interface without receiving an intervening RTI state signal.

Consider exemplary claim 1, which recites in relevant part:

"…receiving a plurality of instructions from a test interface;

loading the plurality of instructions into an emulation instruction register;

…

providing the first instruction to a decoder of the processor if the first instruction is valid;

without receiving a run-test idle state signal, …

providing the second instruction to the decoder if the second instruction is valid." (emphasis added)

None of Shang, Iizuka, and Scantlin teach or suggest, either alone or in combination, receiving multiple instructions from a test interface and providing the instructions to a decoder without receiving an intervening run-test-idle state signal. Accordingly, Applicants submit that independent claims and their dependencies, are allowable.

Enclosed is a check in the amount of $770 for the Request for Continued Examination. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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